AMAURY DARSCH
HIGH PERFORMANCE SOFTWARE ARCHITECT

Personal

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Highest qualification:	PhD in Computer Sciences, INRIA/Rennes University, France

Summary

Fellow computer scientist specialized in the architecture and development of complex systems built around multithreaded, parallel and distributed high-performances computing solutions with a special emphasis on gpu based intelligent computing. Currently working on the development and deployment of a new technology termed “constellation computing”.

Skills

High performance computing	Multi-threaded & distributed system architecture; High-performance, fault tolerant networks; Parallel computing with Vulkan, OpenGL, CUDA and OMP; Quantum computing with IBM Quantum Experience; Low latency bus based data delivery ; 3D rendering with Vulkan, OpenGL and DirectX; Image compression and streaming.
Languages and systems	C, C++, Java, Python, Scheme, Fortran, Assembly; Linux, FreeBSD, Solaris, MacOS, Fedora, Ubuntu, Debian; Parallel and distributed architecture; Complex multi-platforms software design; Original designer of the AFNIX system, http://www.afnix.org.
Networking	Internet protocol V4 and V6; Socket programming and protocols; Distributed operations and file systems; Data replication, feed and streaming systems; Cryptography and security with TLS.
Development	Git, Subversion, CVS, ClearCase; Linux and Windows development environments; Project development operations tools; Agile methodologies, Atlassian tools suite.
Management	International multi-sites project management; Extensive experience of Silicon Valley, Canada and France; Highly experienced complex project architect and manager; General manager and founder of the Ethernix company.

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Professional history

Quantic Dream (Paris, Since May 2022)
http://www.quanticdream.com

Low level engine senior contributor. Responsible for the development and implementation of high-performances mathematical libraries in C++. The mathematical chain is a key element of a gaming experience which interacts with numerous engine, inclusing the physical and rendering engines.

Ethernix (Lorient, Since Dec 2019)
http://www.ethernix.com

Founder of the Ethernix company. Ethernix develops, market and distributes state-of-the-art firm modeling tools platforms that address the increasing needs for the deployment of local or distributed complex simulation platforms. Ethernix is a long term project targeting the deployment of the "Constellation Computing" technology developed from the ground up. The constellation integrates in a single platform several computing models, including gpu compute shaders, browser web assembly and newer quantum computing virtual engine. The platform is currently under test and can be visited at http://www.ethernix.net.

Blade Group (Paris, Dec 2015, Dec 2019)
http://www.blade-group.com

Fellow. Head of software research lab. Original developer of the Shadow product cloud server with an emphasis on low latency, high-quality, high-speed acquisition and encoding facility. Other duties include managing the research lab and following interns from various schools (Telecom Paris, École Polytechnique, Université Paris 6).

CA Corporate & Investment Bank *(Paris La Defense, May 2015, Dec 2015)*
http://www.ca-cib.com

Consultant in the e-trading department for the development and optimization of the feed-handler components of the new e-trading platform. A feed-handler is a critical component that collect financial instrument data and distribute them on the internal bus for further processing by pricing components which are part of an automated tool chain within a financial desk.

Silkan Canada *(Montréal, Canada, Sep 2012, Oct 2014)*
http://www.silkan.com

Lead architect for a high-performance software modeling project centered around a multithreaded and distributed execution core with a strong emphasis on complex numerical computation

- Lead architect of the overall project.
- Designer of the multithreaded execution core.
- Team management and project leadership including control and accountability.
- International coordination with Silkan Meudon and Montpellier.

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Silkan *(Meudon, France, Apr 2010, Sep 2012)*
http://www.silkan.com

Senior software expert. Silkan is a French company based in Meudon, France, specialized in the design of high performances computing platforms. Most of the projects are addressing the very demanding EDA sector by developing and deploying an advanced algebraic computing platform. Main designer of high-performance, thread-safe, parallel computational libraries with OpenMP.

ESILV *(Paris, France, Sep 2007, Jun 2010)*
http://www.esilv.fr

Director of the Information engineering department. ESILV is an engineering school, located in the Léonard de Vinci complex in Paris La Défense. The information engineering department is responsible for the graduation of engineers specially trained in the field of computer sciences.

Ethernix *(Lorient, France, Nov 2005, Jul 2017)*
http://www.ethernix.com

Founder of the Ethernix company. Ethernix develops on demand software solution in the field of high-performance, parallel and distributed computing. Currently working on the "constellation computing" project.

Virtutech *(San Jose, Ca – Jan 2005, Nov 2005)*

Senior software manager for Virtutech, Inc located in San Jose, Ca. The primary duties are to pilot the device modeling operations in the US in relation with the Stockholm research center. Principal duties includes device and machine modeling for a broad range of systems with an emphasis on the embedded kernel simulation or with the full operating system execution.

IRISA *(Rennes, France – Jan 2002, Dec 2004)*
http://www.irisa.fr

PhD student of André Seznec. The PhD thesis title is "out-of-order execution with predicate ISA". In order to attack the problems associated with the out-of-order execution of predicated ISA. The thesis was completed in 35 months.

Cadence Design System *(San Jose – Sep 1998, Sep 2001)*
http://www.cadence.com

Senior member of the consulting staff. Member of the PKS team of the Ambit group of Cadence. The objective was to deliver a new framework which handle multi-million gates design with first time working timing/routing silicon.

Aristo Technology *(Cupertino, Ca – Feb 1997, Sep 1998)*

Principal engineer. Aristo Technology, Inc. Join the company on February 1997. Responsible for the project integration. The project is focusing on the new System-on-a-Chip (SOC) paradigm.

Compass Design *(San Jose, Ca – Jun 1995, Feb 1997)*

Worldwide application manager for the front-end tools. With a small team of corporate engineers, responsible of the Compass synthesis solution, including HDL floorplanning.

Compass Design *(Paris, France - Mar 1993, Jun 1995)*

Eastern countries special operations. Special project engineer working on long term projects with various Compass customers.

Compass Design *(Nice, France - Mar 1991, Mar 1993)*

Special projects ASIC design engineer. The main project included a complete library re-design with 300 standard cells, their adaptation to a low-voltage operation .

VLSI Technology *(Nice, France - Jun 1989, Mar 1991)*

Design engineer. Develop and characterized a 20 MHz version of the Z80 in the VLSI 1.0µm technology.

Business experiences

Ethernix *(Lorient, France, since Nov 2)*
http://www.ethernix.com

Founder of the Ethernix company. Ethernix develops on demand software solution in the field of high-performance, parallel and distributed computing. Currently working on the "constellation computing" project visible at http://www.ethernix.net.

Academic experiences

ESILV *(Paris, France, Sep 2007, Jun 2010)*
http://www.esilv.fr

Director of the Information engineering department. The information engineering department is responsible for the graduation of engineers specially trained in the field of computer sciences.

ESEO Engineering school*(Sep 2002 – Sep 2012 , to Sep 2015)*

Special lecturer for an introduction to the software complexity. Computer Sciences lecturer at ESEO Paris for undergraduate students.

ESIEE *(Paris, France – Sep 1993, Jun 1995),*

Lecturer at Engineering school, ESIEE located in Marne La Vallée, near Paris. The course covered the fundamental of parallel architecture with an emphasis on superscalar implementation.

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Education

IRISA *(Rennes, France – Jan 2002, Dec 2004),*
PhD in Computer Sciences from Rennes University, France.

ESEO *(Angers, France – Sep 1985, Juin 1989),*
MS EE/CS from ESEO, Angers, France.

EASA, FAA
PPL (FRA/USA), IFR(USA), FCL.055 (FRA), CAEA (FRA)